

FIG. 1A

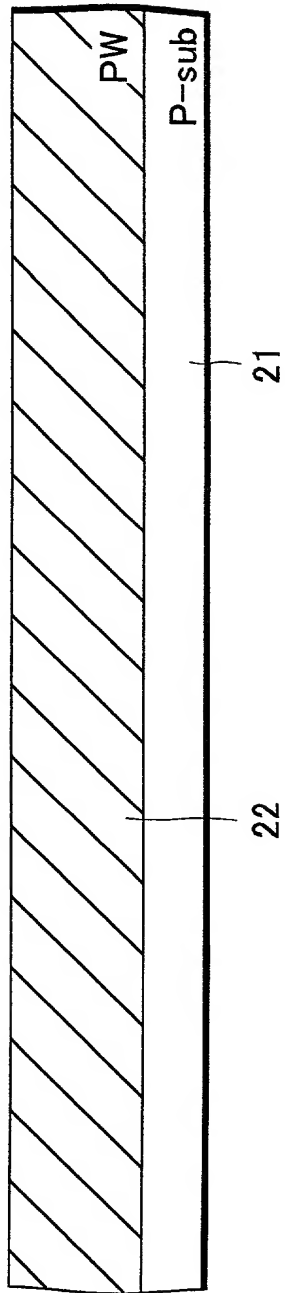
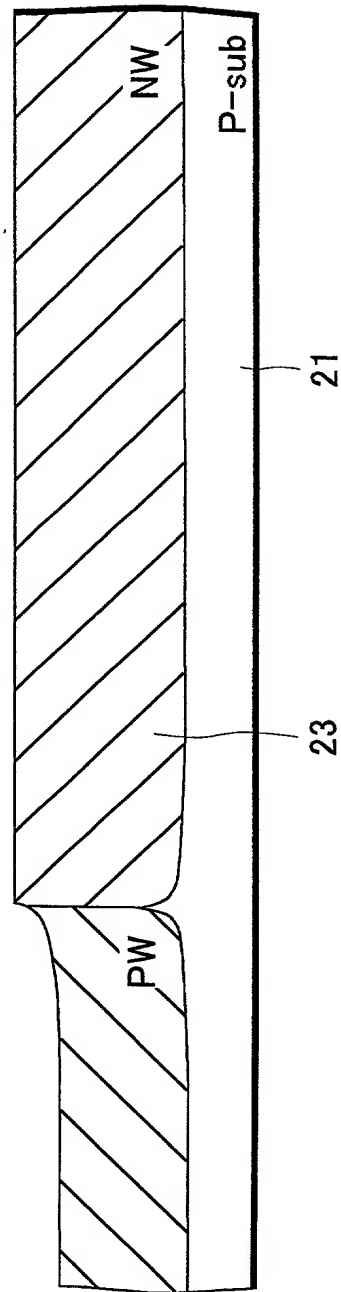


FIG. 1B



This diagram shows a cross-sectional view of a semiconductor device. It features a P-substrate (21) with a P-well (PW) region. A series of regions are formed along the surface, including LN (24) and PR (25) regions, which are separated by a thin layer (26). The regions are labeled with numbers 24, 25, and 26, and the overall structure is labeled P-sub.

FIG.3A

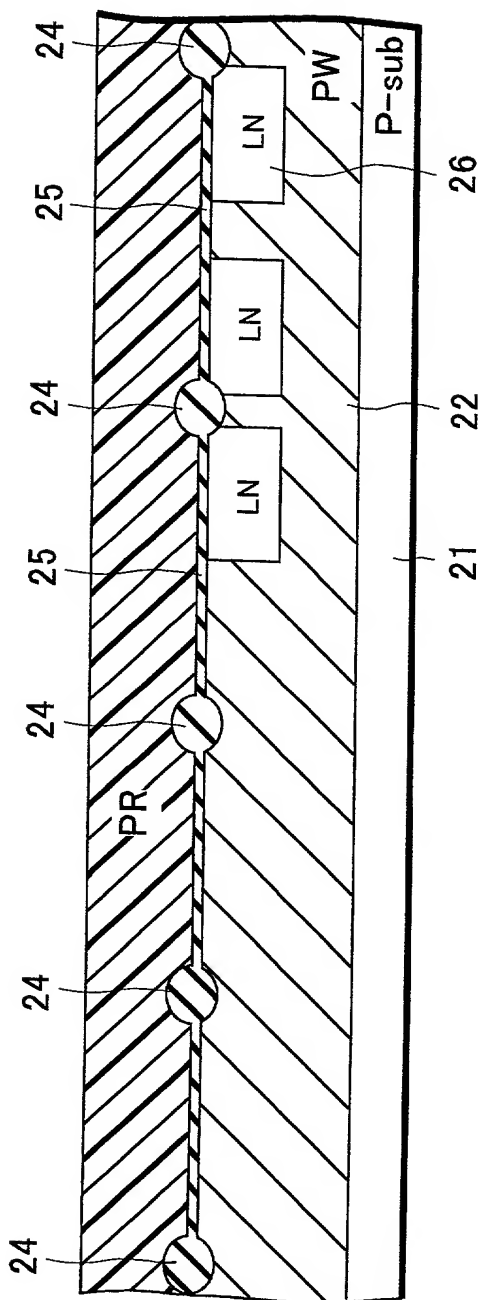


FIG.3B

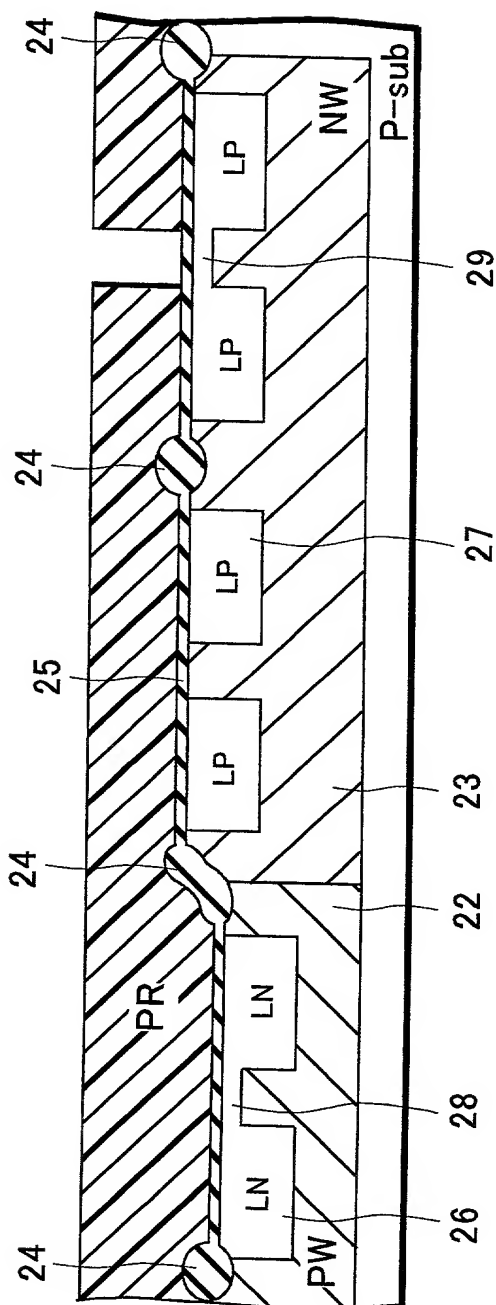


FIG.4A

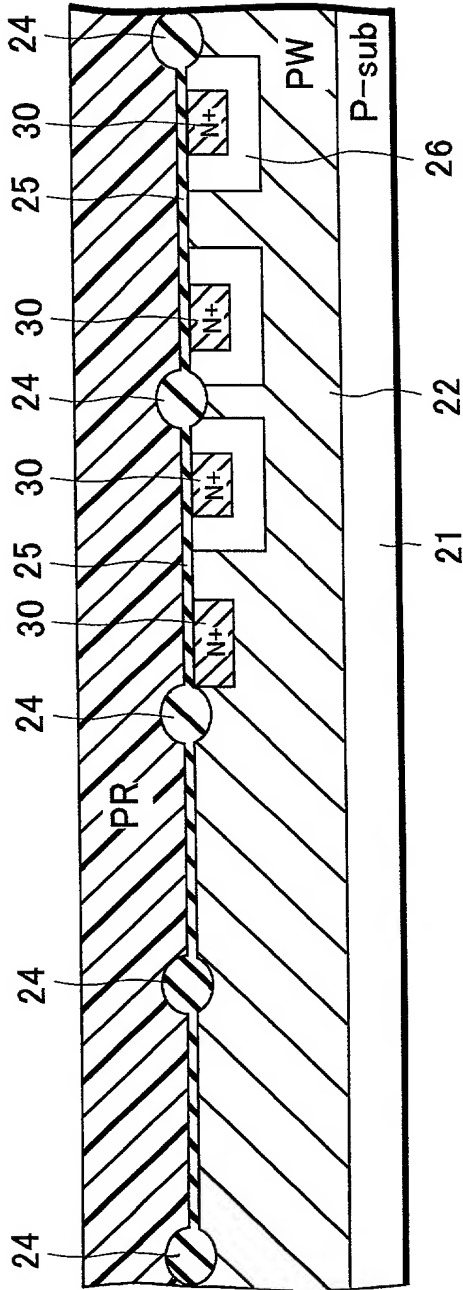
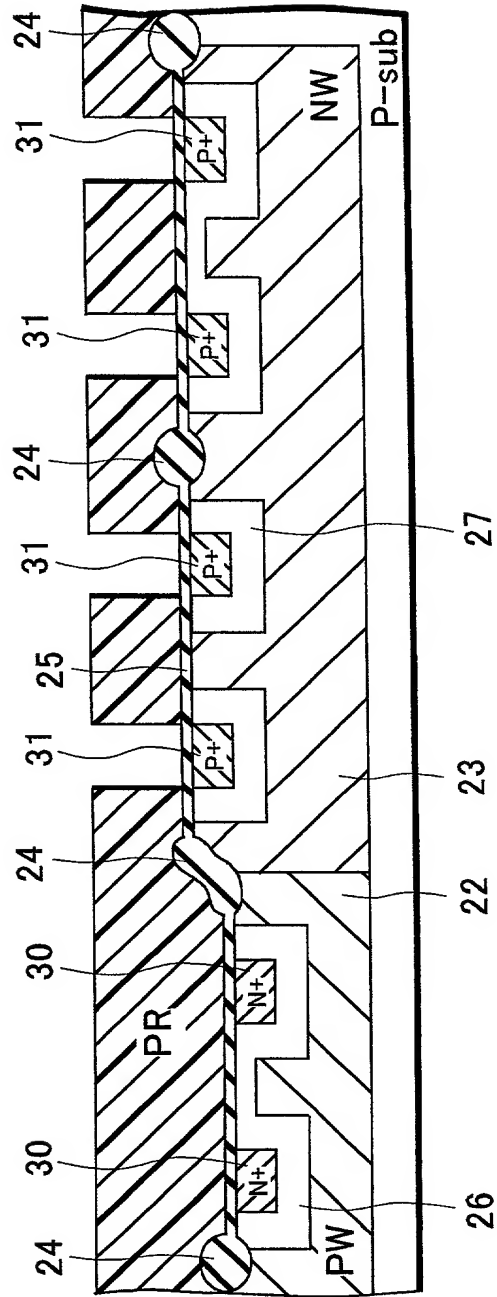


FIG.4B



This cross-sectional view shows a semiconductor device with a substrate 33 and a P-sub layer 32. The device features a series of gates 26, 27, 28, 29, 30, and 31. The gates 26, 27, 28, and 29 are labeled with P+ and N+ regions. The gates 30 and 31 are labeled with P+ regions. The gates 26 and 31 are connected to a common contact 24. The gates 27, 28, and 29 are connected to a common contact 25. The gates 30 and 31 are connected to a common contact 23. The gates 26 and 31 are connected to a common contact 22. The gates 27, 28, and 29 are connected to a common contact 21. The gates 30 and 31 are connected to a common contact 20. The gates 26 and 31 are connected to a common contact 19. The gates 27, 28, and 29 are connected to a common contact 18. The gates 30 and 31 are connected to a common contact 17. The gates 26 and 31 are connected to a common contact 16. The gates 27, 28, and 29 are connected to a common contact 15. The gates 30 and 31 are connected to a common contact 14. The gates 26 and 31 are connected to a common contact 13. The gates 27, 28, and 29 are connected to a common contact 12. The gates 30 and 31 are connected to a common contact 11. The gates 26 and 31 are connected to a common contact 10. The gates 27, 28, and 29 are connected to a common contact 9. The gates 30 and 31 are connected to a common contact 8. The gates 26 and 31 are connected to a common contact 7. The gates 27, 28, and 29 are connected to a common contact 6. The gates 30 and 31 are connected to a common contact 5. The gates 26 and 31 are connected to a common contact 4. The gates 27, 28, and 29 are connected to a common contact 3. The gates 30 and 31 are connected to a common contact 2. The gates 26 and 31 are connected to a common contact 1. The gates 27, 28, and 29 are connected to a common contact 0.

[illegible]

This diagram shows a cross-sectional view of a semiconductor device. It features a P-substrate (27) at the base. Above the substrate, there are several layers and regions: a P+ region (24), an N+ region (31), a P+ region (25), and a NW region (27). A PR layer (23) is also present. Other labeled regions include 24, 31, 25, 27, 23, 22, 30, 32, 26, and PW. The diagram illustrates the complex layering and doping profile of the device.

FIG. 7A

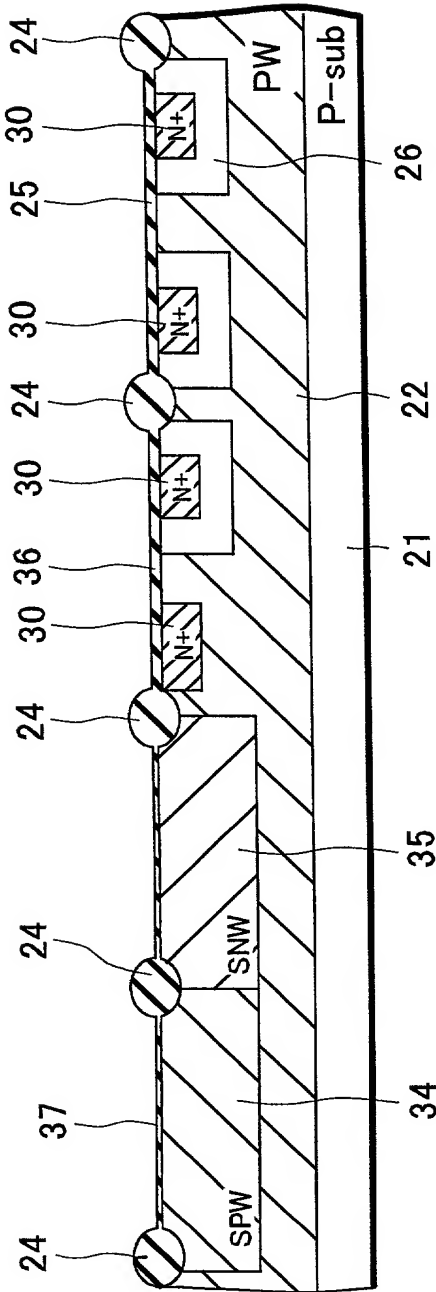


FIG. 7B

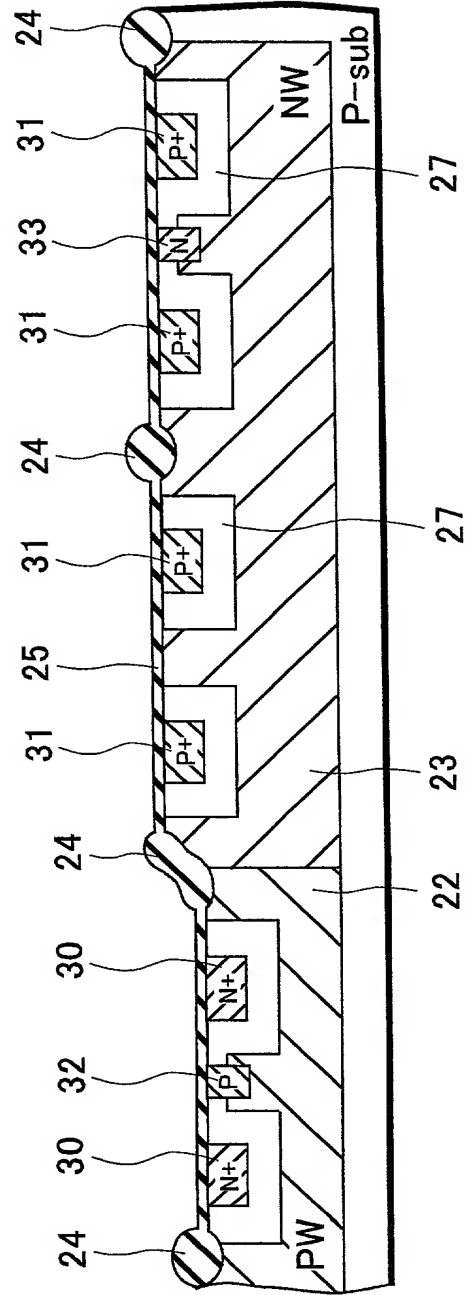


FIG. 8A

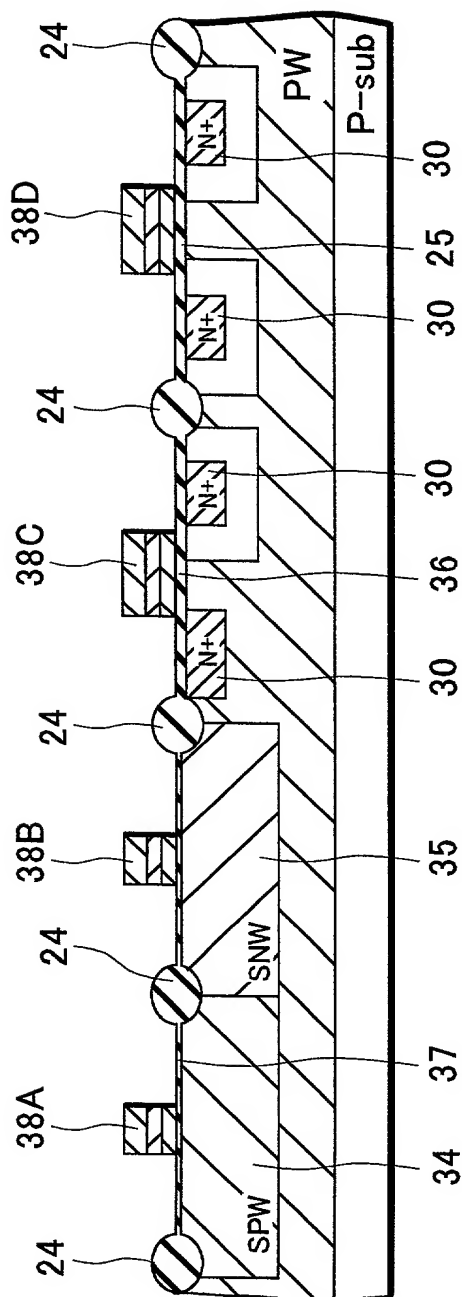
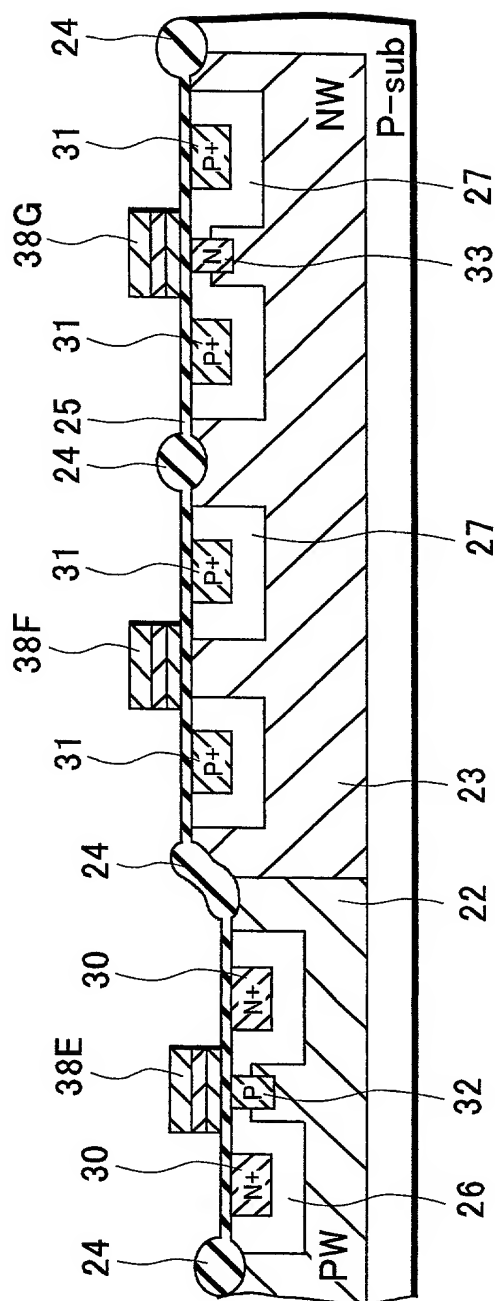


FIG. 8B



This cross-sectional view shows a semiconductor device with a substrate labeled 'P-sub'. The device features several regions: 'SPW' (Semiconductor Patterned Wafer) and 'SNW' (Semiconductor Patterned Wafer) are located at the bottom. Above these are regions labeled 'N-' and 'P-'. The top layer is labeled 'PW' (Passivation Wafer). The device is divided into sections labeled 38A, 38B, 38C, and 38D. The regions are further defined by labels 24, 39, 40, and 30. The regions are separated by vertical lines, and the top surface is covered by a passivation layer.

[illegible]

FIG.10A

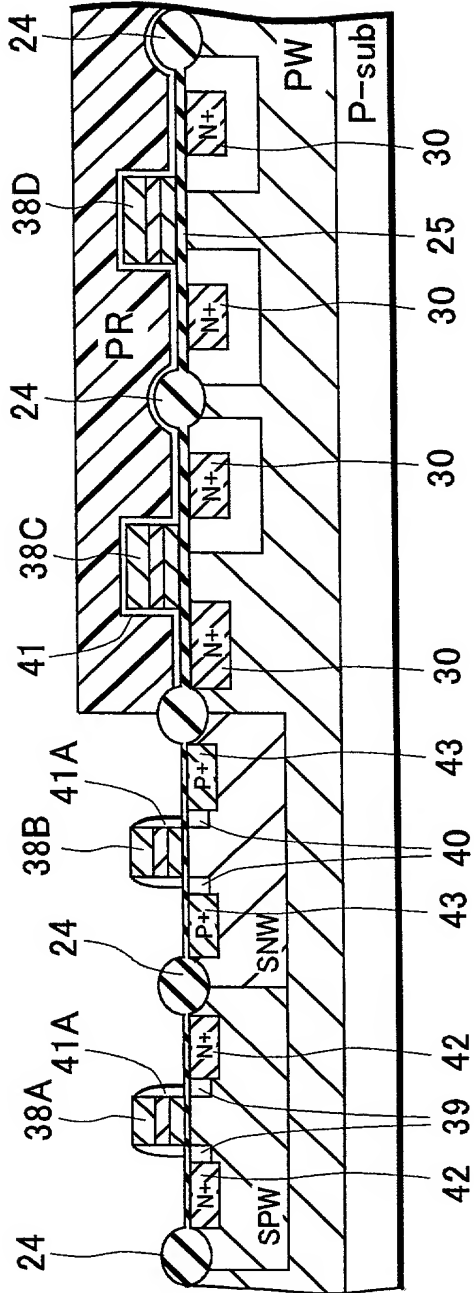


FIG.10B

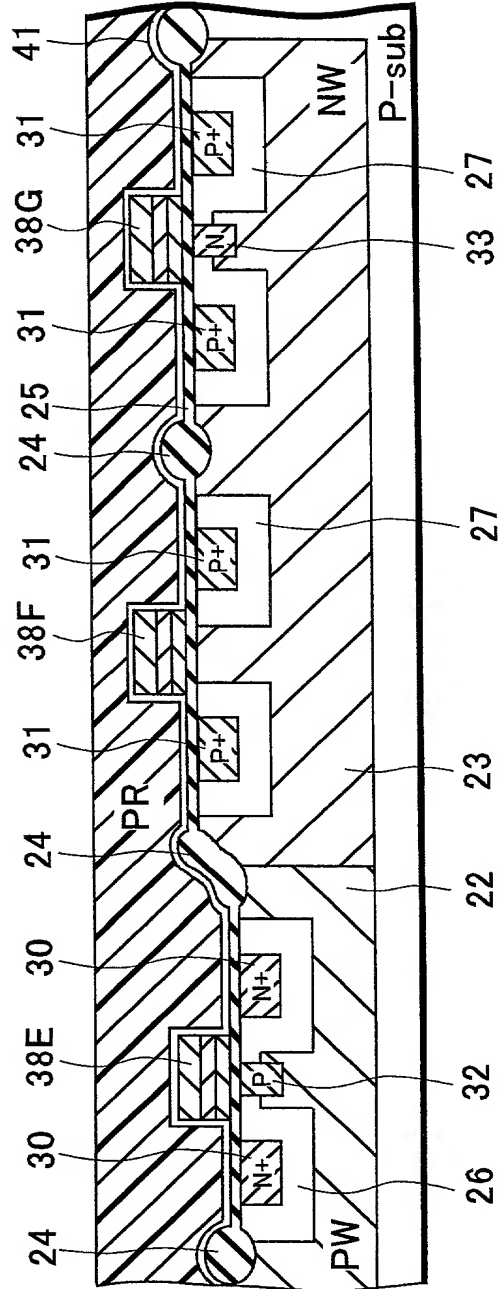


FIG. 11A

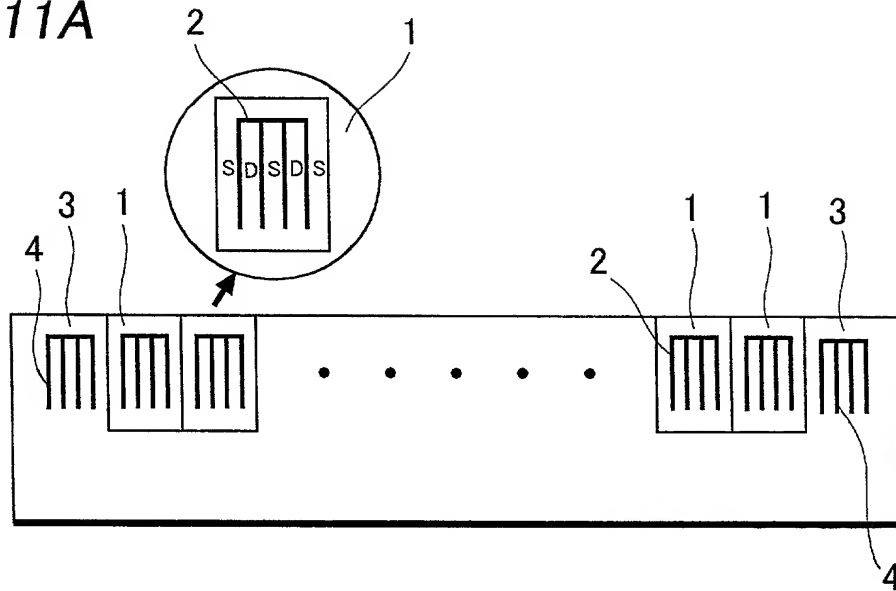


FIG. 11B

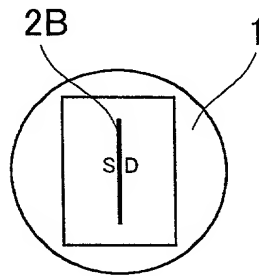


FIG. 11C

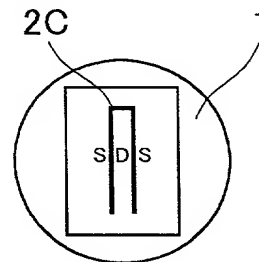


FIG. 11D

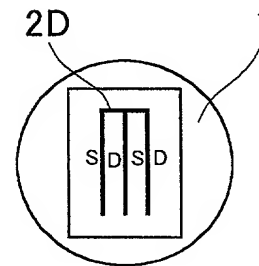


FIG.12

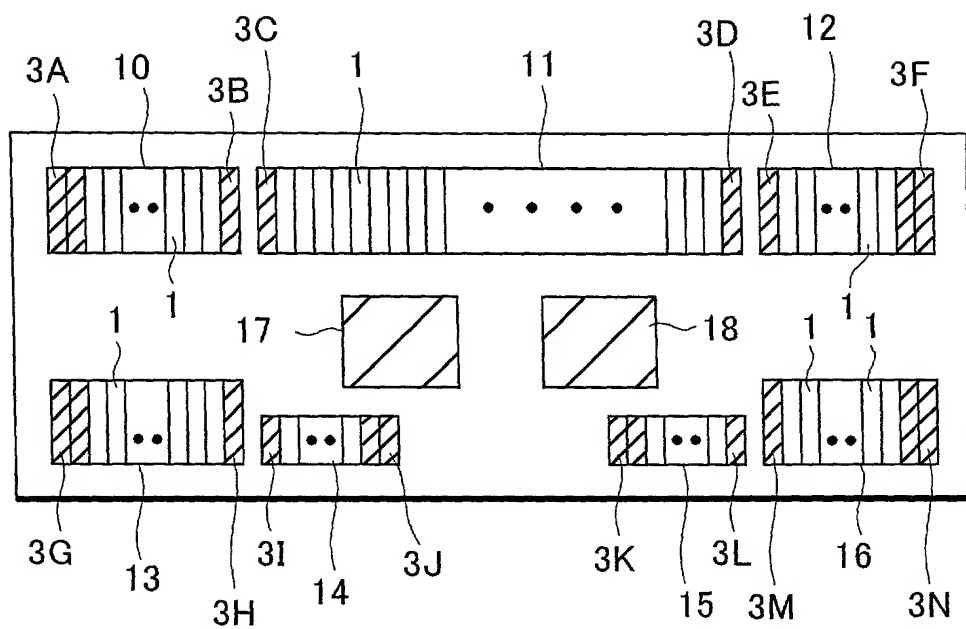


FIG.13

